

ABSTRACT OF THE DISCLOSURE

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A recording/reproducing apparatus comprising an OP head 11, a wobble circuit 12, a system controller 13, and an address-decoding timing generator 14. The wobble circuit 12 extracts a wobble signal from the signal the OP head 11 has read. A PLL circuit for generating a sync signal from the wobble signal is held while no normal wobble signal is generated. The address-decoding timing generator (Address DEC TG) 14 receives a signal the OP head 11 has reproduced, decodes the address represented by the signal, and supplies the address data to the system controller 13. The generator 14 also generates a timing signal from the sync signal supplied from the wobble circuit 12 and supplies the timing signal to the other components of the recording/reproducing apparatus.

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